

Communications Core Meets 3G Wireless Handset Challenges

USE THE LATEST DSP CORE AND SOFTWARE TECHNOLOGY TO SATISFY THE PERFORMANCE AND COST DEMANDS OF 3G APPLICATIONS.

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THIRD-GENERATION (3G) mobile handsets may still be in the prototype stage, but analysts predict that by 2004, global sales of digital cellular handsets will be on the order of \$994 million (Fig. 1). While slated to offer a wide range of services, including voice, data, location assistance, audio, still pictures, and streaming video, these complex and multipurpose devices will form the foundation for applications and services that are yet to be imagined. Unfortunately, the ambiguity of ensuring the commercial success of handsets with these features poses a difficult challenge for the original-equipment-manufacturer (OEM) designer building 3G products for the end consumer.

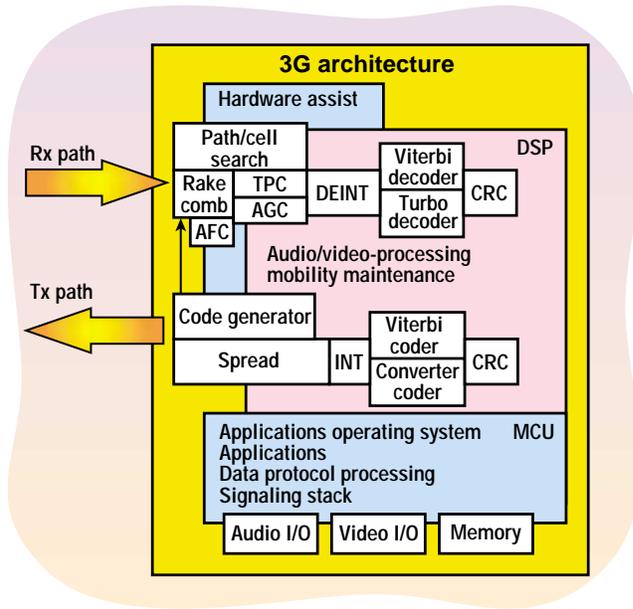
While the consumer market and service providers are enthusiastic about the capabilities and potential revenues related to 3G applications, wireless system designers, on the other hand, need to solve the challenges stemming from the integration of multimedia applications and services into a small, power-efficient, and inexpensive handset. One of the most important components in a 3G handset is the system-on-a-chip (SOC) that handles digital baseband functions, such as speech coding,

error-correction modulation, and demodulation. At the heart of this SOC is the digital-signal-processing (DSP) core.

DSP core vendors must supply four key features to help enable OEM success while, at the same time, satisfy the demands of the 3G-handset market. These demands include the following: efficient C code compilability, high performance, low power consumption, and compact code density.

Having efficient code compilability means that 90 percent or more of the production code must be able to be developed by leveraging the C source code and the compiler associated with the specific DSP core. The benefit of this compilability is that it minimizes the need to hand code in assembly language. The result is the faster time to market needed by OEMs to meet end-customer demand for new applications and value-added features in shorter amounts of time.

With regard to high performance, the complex array of features in 3G handsets requires unprecedented DSP horsepower of up to 3000 million instructions per second (MIPS). This performance must be achieved with very low power consumption per



1. Dataquest projections for the digital cellular handset market are global sales of \$994 million by 2004.

function. Subsequently, new 3G handsets require improvements to the DSP core current drain.

Lastly, in order to keep the overall SOC size at a minimum and the system cost low, the DSP core must feature efficient use of memory. This can best be achieved through compact code density. In other words, having the fewest number of lines of code as possible for a particular application.

MIGRATION CHALLENGES

The evolution of wireless services has gone through many incarnations. In the first generation (1G), analog voice-centric systems that are transitioned into digital systems offer voice plus wireless data rates of less than 14 kb/s. These digital systems are often referred to as second-generation (2G) products. The 2.5G, or transitional generation, includes general- packet radio service (GPRS). It promises data rates of up to 114 kb/s and continuous connections to the Internet for mobile-phone and computer users. Another 2.5G standard, Enhanced Data rates for Global Evolution (EDGE), promises data rates up to 384 kb/s.

The 3G systems set to hit the market are the result of a vision from the International Telecommunications Union (ITU), typically defined as IMT-2000 (now often referred to as 3G). The IMT-2000 specification defines data rates for specific operating environments that can be served by 3G. For instance, with indoor stationary picocells, the minimum data rate is 2 Mb/s; for the local pedestrian microcell, the minimum data rate is 384 kb/s; and for the regional or vehicular macrocell, the minimum rate is 144 kb/s. In all of these cells, the 3G system needs to simultaneously support multiple types of traffic, including high-speed Internet, two-way video, images, voice, and location services.

3G systems, enabled by technologies, such as cdma2000 and wideband code-division multiple access (WCDMA), will allow handset users to connect to the Internet/Intranet at data rates described earlier. Higher data rates are not the only defining specification of 3G wireless. In fact, 3G systems will increase voice capacity up to two times, employing 8-phase-shift-keying (8-PSK) and quadrature-phase-shift-keying (QPSK) modulation schemes.

The 3G handset needs to accommodate and manipulate multiple protocols and technologies to manage the various

3G HANDSETS WILL USE BLUETOOTH TECHNOLOGY FOR THINGS, SUCH AS SHORT-RANGE NETWORK COMMUNICATIONS, HANDWRITING RECOGNITION, VOICE RECOGNITION, MMC SUPPORT, AND TEXT-TO-VOICE TECHNOLOGIES.

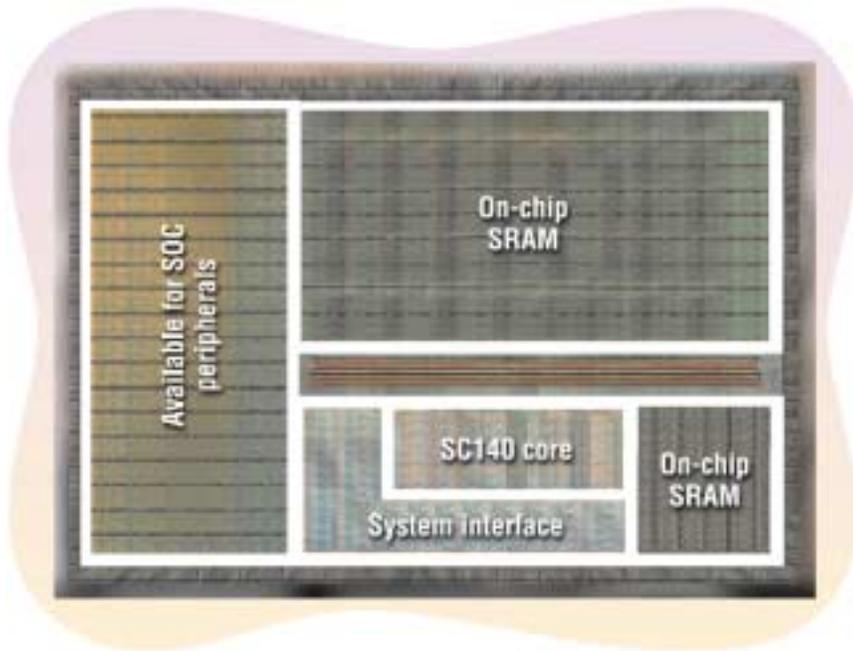
types of multimedia data required to send and receive. Some of the latest technologies that 3G will take advantage of include Motion Pictures Experts Group audio layer 4 (MPEG-4) for video, MPEG-3 for audio, voice over Internet Protocol (VoIP) for low-cost long-distance voice, and Joint Photographic

Experts Group (JPEG). JPEG2000 for still pictures and a series of rapid still pictures will also be valuable.

Future 3G handsets will use encryption technology for security and financial e-commerce-type transactions. Location services such as Global Positioning Systems (GPS) and enhanced-911 (E-911) will also play an important role in future handsets. Additionally, 3G handsets will use Bluetooth technology for things, such as short-range network communications, handwriting recognition, voice recognition, multimedia-card (MMC) support, and text-to-voice technologies.

What does all of this mean for the DSP core? Consider for a moment that higher data rates and the explosion of new 2.5G and 3G user features will necessitate greater DSP processing capabilities in terms of single-cycle multiply accumulates (MACs) or MIPS. As a result, DSP cores with performance under 1000 MIPS will not be well-suited for high-end 3G applications, since they will require extensive hardware assist to meet the new performance demands. Conse-

DSP CORES



2. A typical 3G multicore architecture for a WCDMA baseband solution featuring a DSP core, a microcontroller, and additional application-specific intellectual property is shown here.

quently, the need for extensive hardware assist will reduce programming flexibility.

Since 3G specifications are still in flux and all of their potential applications not well-defined yet, the digital baseband functionality will need to be highly programmable. In other words, it must be software rather than hardware. This will provide system designers with the capability to make rapid changes in a programming friendly environment. As market demands and standards solidify, OEMs can then program/reprogram the DSP core quickly within shrinking product-design cycles. In addition to performance and flexibility, the DSP core for 3G handsets also needs to be extremely efficient in its consumption of power. For instance, a 10-fold increase in processor performance needs to be matched by at least a 10-fold improvement in milliwatt/MIPS of power consumed.

Perhaps one of the greatest challenges for DSP cores targeting 3G handsets is the ability for designers to adequately manage size and cost of the digital baseband functionality—which is directly related to DSP code density. To quantify the challenge, note that the number of lines of C code in a 3G handset is expected to be more than 10 times that of a 2G phone. This means that DSP cores must be as efficient as possible to minimize the need for memory for a particular application.

Overcoming this challenge is especially crucial because memory takes the largest amount of space on the SOC device that handles the digital baseband functionality. As a result, DSP cores with compact code density translate to lower overall system cost in the 3G handset. Also, compact code density can eliminate the need for off-chip memory to support digital baseband functionality. This reduces not only handset chip count and size, but the power consumed moving data between different chips as well. The net result is that the end user receives a small, lightweight, and more-affordable handset with longer battery life.

CORE TECHNOLOGY

The high-performance demands of 3G products can be effectively dealt with using a system architectural approach that encompasses a DSP paired with a reduced-instruction-set-computer (RISC) microcontroller unit (MCU). With this approach, major system tasks can be partitioned into the primary elements of the SOC product (Fig. 2) including a DSP core, such as the StarCore SC140.

The StarCore SC140 product is a 16-b retargettable core from StarCore Technology Center—a Lucent Technologies Microelectronics Group and Motorola Semiconductor Products Sector joint design center in Atlanta, GA. Other key elements of the SOC product are an MCU

and a few specialized hardware assists. Intellectual-property blocks can be included that come from the OEM or the SOC vendor, implemented in either hardware or DSP software.

Functions such as higher-level protocol layers and application operating systems (OS) are supported by an MCU. One example is the MCore MCU core from the Motorola Semiconductor Products Sector. This core has been cross-licensed to the Lucent Technologies Microelectronics Group. Other industry RISC MCU cores can be coupled with the SC140 DSP core in SOC products as well.

The primary functions of the DSP core include mobility maintenance and audio/video processing. Depending on the application, the DSP core must also be capable of handling inputs from a mixture of hardware and software. And it must enable the operation of functions such as coding and decoding, voice recognition, and customized MPEG-4. Although MPEG-4 is a standard, it allows implementers a high degree of differentiability through error resiliency and error recovery. This differentiation can be easily implemented in DSP software.

At its most basic level, a DSP core for 3G needs to support Layer 1 functions. These functions include vocoders that are part of every wireless standard and channel encoders, such as Viterbi and Turbo. It must also support MPEG-4 encode and decode, JPEG2000, MP3 audio processing, and speech recognition. A good DSP core can provide the wide range of functions necessary through robust software capabilities with minimal use of additional hardware. Implementing functions in software supports greater programming flexibility and takes up less chip real estate.

The amount of channel coding—required for error correction—when transitioning from 2G to 3G handsets will increase approximately 15-fold. Keep in mind, this number will depend on the system and data rate. As an example, consider a 2G Global System for Mobile Communications (GSM) system. Suppose the system employs a TCH/FS channel type with Viterbi decode constraint length $K = 5$, a code rate of $R = 1/2$, and a block length and data rate of 189 at 20 ms. Assume also that it requires 1940 SC140 cycles per block, which translates into 0.097 SC140 millions of cycles per second.

Historically, 2G channel coding could

not be performed on a DSP. Designers employed additional costly hardware in order to execute this operation. In 3G applications, with higher data rates than 2G, a WCDMA data channel employing Turbo coding with a data rate of 64 kb/s will only require approximately 15 percent of the SC140's capability. The SC140 was specifically designed with the performance headroom needed to support multimode capabilities and future multimedia applications.

In order to handle the anticipated performance needs of 3G, the DSP core must meet performance requirements up to 3000 MIPS. This represents a significant leap from the 100 MIPS or less that is required by 2G wireless handsets. The SC140 core achieves this level of performance through a parallel architecture (Fig. 3). In a single clock cycle, the SC140 core can execute two address-generation-unit (AGU) instructions and four MAC instructions, leading to performance of 3000 RISC MIPS/1200 million MACs (MMACs) at 300 MHz.

In addition to thousands of MIPS, the DSP core for 3G will require more lines of code to support the rich 3G-handset feature set, while satisfying frugal power-budget constraints. In fact, the DSP core must consume less than it did at 2G, while performing approximately 10 times the work. As a result, DSP core vendors must improve power consumption per instruction burned for next-generation wireless handsets.

In response, some of the latest DSP cores have been designed with ultra-low

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power consumption. For instance, using current process technologies, the SC140 consumes an estimated 198 mW of peak power while operating at 300 MHz, or 1200 MMACs (3000-RISC MIPS) at +1.5 VDC for high-end 3G handsets. At +0.9 VDC, performance of 120 MHz, or 480 MMACs (1200 RISC MIPS), is maintained with peak power of 28 mW. The +0.9-VDC option, designed for lower-end 3G phones where performance is less critical, conserves even more battery life.

Having a programmable, flexible, and scalable DSP core solution enables fast time to market. For instance, if the same DSP code can be reused from 2G to 3G and span handsets to infrastructure, OEMs can get products to market much faster—giving them a competitive edge.

In addition, if the DSP core can be quickly retargeted to different manufacturing processes, such as with the StarCore Design System (SCDS) methodology, the core can be manufactured using the optimal process in terms of performance and cost for a given application.

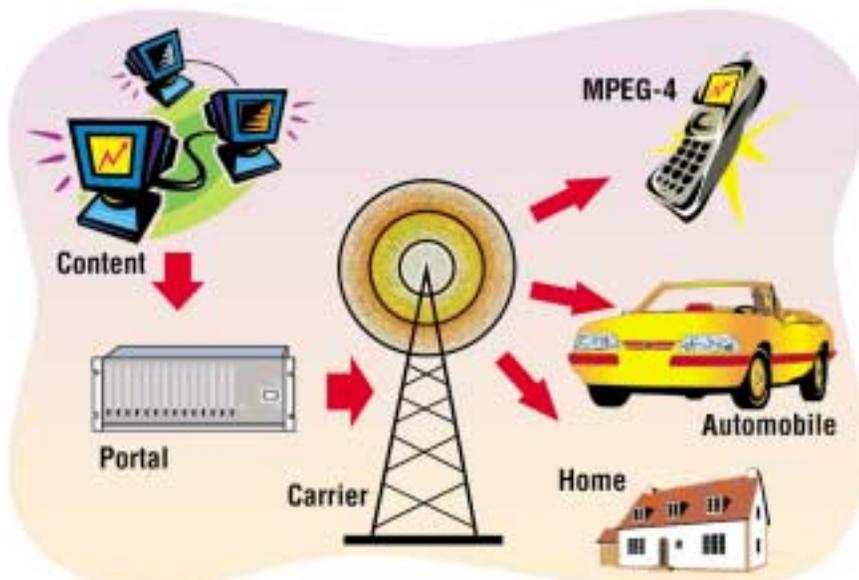
In fact, lower system cost is directly related to the size of the core and efficiency of the DSP core with respect to software code density. Efficiently compiled and optimized code can reduce the amount of software required for a particular application, thus shrinking the SOC device size and reducing overall system cost.

AN EXAMPLE

One feature that distinguishes 3G from its predecessors is the ability to handle video-processing applications. This is perhaps the most challenging application for the new handsets. Video processing on a DSP for use in a mobile environment requires an increased need for MIPS, while still possessing the low-power budget and a very-challenging radio channel that comes with its associated disturbances and losses.

MPEG developed a family of standards to define the coding of audiovisual information in a digital compressed format. MPEG-4, specifically developed for wireless environments, takes the special challenges into account faced by wireless transmission, such as multipath fading. It provides error robustness and resilience to enable streaming video transmissions over the challenging medium of the radio channel and the Internet. Additionally, it enables various types of mobile services at bit rates ranging from 10 kb/s to 2 Mb/s and addresses the challenges of delivering wireless video communications over a wide range of bit rates on a potentially error prone, low-bit-rate medium such as those provided by mobile radio channels. As a result, MPEG-4 is attractive for 3G applications where less bandwidth may be available due to heavy voice and/or data traffic.

For wireless video, content is encoded and sent to a server through a public-switched telephone network (PSTN). Content can include pre-encoded video clips, one-way streaming video, or two-way real-time videoconferencing. Then it is delivered to the subscriber through a digital wireless carrier. At the subscriber unit, such as a 3G handset, a DSP employing MPEG-4 technology decodes the signal for viewing.



3. The SC140 DSP core from StarCore features a parallel architecture, which allows it to deliver the 3000-RISC MIPS required by high-end 3G applications.

DSP CORES

Traditionally, real-time video coding and decoding was not implemented on a DSP due to the lack of processing power and memory bandwidth for memory processing. However, a DSP core, such as the SC140, is unique because it provides the high performance as well as the memory capability to enable video processing.

The SC140 is equipped with four data arithmetic logic units (ALUs) and two address-generation units (AGUs), offering inherent data parallelism. This enables the core to handle the computational complexity required by MPEG-4, such as inverse discrete cosine transform (IDCT), inverse quantization, motion compensation, color-space conversion, and miscellaneous block operations. The four data ALUs (which enable the parallel four MAC capability) on the SC140 run independently and execute the set of instructions required for video processing.

Two 64-b data buses provide the data bandwidth required to keep the four data ALUs fully occupied. While the data ALUs and AGUs in the SC140 core supply the performance required for video processing, the SOC product also needs to have the memory to support the MIPS required by video processing. For an MPEG-4 decoder with a configuration of common intermediate format (CIF), 15 f/s, and 128 kb/s, the loading on the SC140 is less than 20 percent of its total performance budget.

SUMMING IT UP

There is little doubt today that the world is on the verge of 3G deployment. As such, it is truly an exciting time for consumers, service providers, operators, OEMs, as well as SOC device designers alike. The DSP will play a crucial role in addressing the key needs of the 3G wireless market—today and well into the future. In fact, for many, the DSP core will be a defining factor when determining a product's overall competitive advantage. If implemented properly, it will essentially enable OEMs with the ability to rapidly deliver cost-effective, high-performance, low-power solutions. **WSD**

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